

WHAT IS CLAIMED IS:

- 1 1. A method of forming a source/drain of a transistor, comprising:
2 forming a recess in a substrate adjacent a gate of said transistor;
3 forming a deep doped region below a bottom surface of said recess; and
4 epitaxially growing a semiconductor material within said recess to form said
5 source/drain.
- 1 2. The method as recited in Claim 1 further comprising forming a lightly doped
2 drain region adjacent said gate.
- 1 3. The method as recited in Claim 1 wherein said semiconductor material is silicon.
- 1 4. The method as recited in Claim 1 wherein said forming said deep doped region is
2 performed by an ion implantation process.
- 1 5. The method as recited in Claim 4 wherein said ion implantation process
2 comprises implanting one of P-type ions and N-type ions.

- 1 6. A transistor, comprising:
2 a gate formed on a substrate; and
3 a source/drain formed in a recess of said substrate adjacent said gate and
4 including:
5 a lightly doped drain region adjacent said gate, and
6 a deep doped region below a bottom surface of said recess.
- 1 7. The transistor as recited in Claim 6 further comprising another source/drain
2 formed in another recess of said substrate adjacent said gate and including:
3 a lightly doped drain region adjacent said gate; and
4 a deep doped region below a bottom surface of said another recess.
- 1 8. The transistor as recited in Claim 6 wherein said source/drain comprises an
2 epitaxially grown semiconductor material.
- 1 9. The transistor as recited in Claim 6 further comprising spacers on opposing walls
2 of said gate.
- 1 10. The transistor as recited in Claim 6 wherein said gate and source/drain comprise a
2 contact.

- 1 11. A method of forming a transistor, comprising:
2 providing a gate on a substrate, including:
3 forming a gate dielectric over said substrate, and
4 forming a gate electrode over said gate dielectric; and
5 providing a source/drain, including:
6 forming a recess in said substrate adjacent said gate,
7 forming a deep doped region below a bottom surface of said recess; and
8 epitaxially growing a semiconductor material within said recess to form
9 said source/drain.
- 1 12. The method as recited in Claim 11 wherein said providing said source/drain
2 further includes forming a lightly doped drain region adjacent said gate.
- 1 13. The method as recited in Claim 11 wherein said semiconductor material is silicon.
- 1 14. The method as recited in Claim 11 wherein said forming said deep doped region
2 is performed by an ion implantation process.
- 1 15. The method as recited in Claim 14 wherein said ion implantation process
2 comprises implanting one of P-type ions and N-type ions.
- 1 16. The transistor as recited in Claim 11 further comprising providing another
2 source/drain, including:
3 forming another recess in said substrate adjacent said gate;
4 forming a deep doped region below a bottom surface of said another recess; and

5 epitaxially growing a semiconductor material within said another recess to form
6 said another source/drain.

1 17. The method as recited in Claim 16 wherein said providing said another
2 source/drain further includes forming a lightly doped drain region adjacent said gate.

1 18. The method as recited in Claim 16 wherein said semiconductor material is silicon.

1 19. The method as recited in Claim 11 wherein said providing said gate further
2 includes forming spacers on opposing walls of said gate dielectric and gate electrodes.

1 20. The method as recited in Claim 11 wherein said providing said gate and said
2 source/drain further include performing a salicide process to form contacts thereon.